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ATTORNEY DOCKET NO. **10030444-1**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): David D. Balhiser, et al.

Serial No.: 10/728,604 **Examiner:** Wells, Kenneth B.

Filing Date: December 5, 2003 **Group Art Unit:** 2816

Title: DRIVER-SIDE CURRENT CLAMPING WITH NON-PERSISTENT CHARGE BOOST

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on January 3, 2006 .

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
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☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **50-3718** the sum of $500.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-3718** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

☒ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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☐ I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Date of Facsimile:

Typed Name: Gregory W. Osterloth

Signature:

Respectfully submitted,

David D. Balhiser, et al.

By

Gregory W. Osterloth
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Reg. No. 36,232

Date: March 3, 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/728,604	Confirmation No. 9769
Appellants	:	David D. Balhiser, et al.	
Filed	:	December 5, 2003	
TC/A.U.	:	2816	
Examiner	:	Wells, Kenneth B.	
Docket No.	:	10030444-1	

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APPEAL BRIEF

Table of Contents

Section:

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APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Final Office Action dated November 1, 2005.

Appellants filed a Notice of Appeal on January 3, 2006.

Real Party in Interest

The real party in interest is Avago Technologies General IP (Singapore) Pte. Ltd. (Company Registration No. 200512430D), a company incorporated under the laws of Singapore whose registered office is at 8 Cross Street, #11-00 PWC Building, Singapore 048424.

Related Appeals and Interferences

There are no related appeals and/or interferences.

Status of Claims

Claims 1-3, 5, 7-14, 16-21 and 23 remain pending. A copy of the claims is attached as a Claims Appendix to this Appeal Brief. All of the rejections of these claims are appealed.

Status of Amendments

All amendments have been entered.

Summary of Claimed Subject Matter

In a first embodiment (claim 1), a driver circuit (par. [0017], p. 5, line 11 - p. 6, line 6; FIG. 3, 300; FIG. 4, 400; FIG. 6, 600) comprises 1) a first current path (FIG. 3, 302) coupled to a first voltage; 2) a first switching circuit (par. [0019], p. 6, line 13 - p. 7, line 1; FIG. 3, 306; FIG. 4, 402; FIG. 6, 402), under control of an input signal, to couple and uncouple the first current path to an output of the driver circuit; 3) a first current clamp (par. [0020], p. 7, lines 2-9; FIG. 3, 310; FIG. 4, 408; FIG. 4, 416), coupled in the first current path, to prevent a voltage at the output of the driver circuit from reaching said first voltage; 4) a delay circuit (par. [0025]-[0026], p. 10, lines 1-22; FIG. 6, 604), coupled to the output of the driver circuit; and 5) a first non-persistent charge boost circuit (par. [0020], p. 7, line 2 - p. 8, line 3; FIG. 4, 410; FIG. 6, 602), to increase a rate at which the output of the driver circuit switches toward the first voltage when the first current path is coupled to the output of the driver circuit, wherein the charge boost circuit comprises a field effect transistor (par. [0025], p. 9, line 17 - p. 10, line 17; FIG. 6, 602) that is i) coupled in parallel with the first current clamp via its source and drain terminals, and ii) has its gate coupled to an output of the delay circuit.

In a second embodiment (claim 14), a driver circuit (par. [0017], p. 5, line 11 - p. 6, line 6; FIG. 3, 300) comprises 1) a first current path (FIG. 3, 302) coupled to a first voltage; 2) first switching means (FIG. 3, 306; e.g., the "switching circuit", FIG. 4, 402) to couple and uncouple the first current path to an output of the driver circuit; 3) first current clamping means (FIG. 3, 310; e.g., the "current clamp", FIG. 4, 408), coupled in the first current path, to prevent a voltage at the output of the driver circuit from reaching said first voltage; 4) delay means (par. [0025]-[0026], p. 10, lines 1-22; e.g., the "delay circuit", FIG. 6, 604), coupled to the output of the driver circuit; and 5) first non-persistent charge boost means (FIG. 3, 314), to increase a rate at which the output of the driver circuit switches toward the first voltage when the first current path is coupled to the output of the driver circuit, wherein the charge boost means comprises a field effect transistor that is i) coupled in parallel with the first current

clamping means via its source and drain terminals, and ii) has its gate coupled to an output of the delay means.

In a third embodiment (claim 17), a method (par. [0012], p. 3, line 13 - p. 4, line 1; FIG. 1, 100) comprises, under control of an input signal, driving a signal line toward a first voltage by coupling (FIG. 1, 102) a first current path to the signal line. While the first current path is coupled to the signal line, 1) current flow through the signal line is clamped (par. [0013], p. 4, lines 5-10; FIG. 1, 106) by means of a series-connected resistor in the first current path, to prevent the voltage on the signal line from reaching the first voltage; and 2) a non-persistent charge boost is provided (par. [0013], p. 4, lines 2-5; FIG. 1, 104) to the signal line by means of a field effect transistor that is i) coupled in parallel with said resistor via its source and drain terminals, and ii) has a gate that is driven by a delayed version of the voltage on the signal line, to increase a rate at which a voltage on the signal line switches toward said first voltage.

Grounds of Rejection to be Reviewed on Appeal

Whether claims 1-3, 5, 7-14, 16-21 and 23 should be rejected under 35 USC 103(a) as being unpatentable over Hisaka (US Pat. No. 5,334,889) in view of Williams et al. (US Pat. No. 3,798,471).

Argument

Claims 1-3, 5, 7-14, 16-21 and 23 should not be rejected under 35 USC 103(a) as being unpatentable over Hisaka (US Pat. No. 5,334,889) in view of Williams et al. (US Pat. No. 3,798,471; hereinafter "Williams").

Appellants' claim 1 recites:

1. A driver circuit, comprising:
a first current path coupled to a first voltage;
a first switching circuit, under control of an input signal, to couple and uncouple the first current path to an output of the driver circuit;
a first current clamp, coupled in the first current path, to prevent a voltage at the output of the driver circuit from reaching said first voltage;
a delay circuit, coupled to the output of the driver circuit; and
a first non-persistent charge boost circuit, to increase a rate at which the output of the driver circuit switches toward the first voltage when the first current path is coupled to the output of the driver circuit, wherein the charge boost circuit comprises a field effect transistor that is i) coupled in parallel with the first current clamp via its source and drain terminals, and ii) has its gate coupled to an output of the delay circuit.

(Emphasis added)

In rejecting this claim, the Examiner asserts:

. . .note Fig. 1 of Hisaka, which shows a first switching circuit (the PFET within inverter 13), a first current clamp (R10), a delay circuit (inverters 14 and 15) and a FET (Tr15) is parallel with the resistor. Not shown is the parallel capacitor but such would have been obvious in view of the above-noted teachings of Williams et al. The motivation for adding such a capacitor in parallel with the resistor R10 is to increase the switching speed of the PFET within inverter 13 (as taught by Williams et al).

1/13/2005 Office Action, sec. 6, p. 6.

Appellants respectfully disagree.

Although Hisaka teaches a FET (Tr15) in parallel with a resistor (R10), appellants note that Hisaka's FET (Tr15) is not part of a "non-persistent charge boost

circuit", as is the FET recited in appellants' claim. Rather, Hisaka states:

> As the level of the input signal S11, which is applied to the input electrode of the inverter circuit 13, shifts from a high to low level in the output buffer circuit of the above-described construction at a moment t0 as shown in (A) of FIG. 2, an output node n13 of the inverter circuit 13 rises from earth to the power source level as shown in (B) of FIG. 2. Since the fourth and fifth transistors Tr14, Tr15 are both in an off-state at this moment, ***the rising time of the node 13 takes an integrated form due to operation of the resistor R10 and the capacitor C10 and the voltage of the node n13 rises gradually*** as illustrated in (B) of FIG. 2.
>
> Hisaka, col. 3, lines 20-31 (emphasis added).

Thus, Hisaka's FET (Tr15) operates differently, and performs a different function, than the FET recited in appellants' claim 1. That is, Hisaka's delay circuit 14, in combination with the inverter circuit 15, serves to bias FET Tr15 to an "off-state" at the time input signal S11 switches from a high level to a low level. As a result, Hisaka's FET Tr15 does not operate as a "non-persistent charge boost circuit" (like the FET recited in appellants' claim 1). On the other hand, the driver circuit recited in appellants' claim 1 comprises "a first non-persistent charge boost circuit, ***to increase a rate at which the output of the driver circuit switches toward the first voltage***". Thus, Hisaka's FET Tr15 operates differently, and performs a different function, than the FET recited in appellants' claim 1.

In the Final Office Action mailed 11/1/2005, the Examiner admits/asserts:

> . . .While applicant is correct that the voltage of node N13 rises gradually during a portion of the waveform in Hisaka's Fig. 2, there is also a portion of this waveform n13 which increases (i.e., the portion following the gradually increasing portion). Therefore, the above-noted limitation is still met by Hisaka. . .
>
> 11/1/2005 Final Office Action, sec. 4, pp. 2-3.

Appellants believe the Examiner's above position is akin to arguing that, "Racehorse 'X' would have won the race had he not stumbled as he left his gate." This observation, however, does not alter the fact that racehorse 'X' actually lost the

race. In the case at hand, appellants' claim 1 recites "a first non-persistent charge boost circuit, ***to increase a rate at which the output of the driver circuit switches*** toward the first voltage when the first current path is coupled to the output of the driver circuit". When Hisaka's first current path is coupled to the output of Hisaka's driver circuit, Hisaka's FET (Tr15) initially does nothing, thereby causing the voltage at the node n13 to rise "gradually".

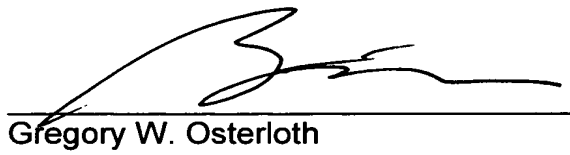
As to Williams teaching a "parallel capacitor", appellants note that a capacitor is not recited in their claim 1. And, although their claim 3 does recite a capacitor, Williams fails to teach that which is missing from Hisaka, as noted in the preceding paragraphs.

Appellants' claim 1 is believed to be allowable over Hisaka's and Williams' combined teachings for at least the above reasons. Claims 14 and 17 are believed to be allowable for similar reasons. Claims 2, 3, 5, 7-13, 16, 18-21 and 23 are believed to be allowable at least because they depend from one of claims 1, 14 or 17, or for reasons similar to why claim 1 is believed to be allowable.

2. Conclusion

In light of the above arguments, Appellants request the allowance of their pending claims.

Respectfully submitted,
DAHL & OSTERLOTH, L.L.P.

By: 

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Claims Appendix

Claim 1: A driver circuit, comprising:

a first current path coupled to a first voltage;

a first switching circuit, under control of an input signal, to couple and uncouple the first current path to an output of the driver circuit;

a first current clamp, coupled in the first current path, to prevent a voltage at the output of the driver circuit from reaching said first voltage;

a delay circuit, coupled to the output of the driver circuit; and

a first non-persistent charge boost circuit, to increase a rate at which the output of the driver circuit switches toward the first voltage when the first current path is coupled to the output of the driver circuit, wherein the charge boost circuit comprises a field effect transistor that is i) coupled in parallel with the first current clamp via its source and drain terminals, and ii) has its gate coupled to an output of the delay circuit.

Claim 2: The driver circuit of claim 1, wherein the first current clamp comprises a resistor.

Claim 3: The driver circuit of claim 2, wherein the first non-persistent charge boost circuit comprises a capacitor, coupled in parallel with said resistor.

Claim 4 (canceled)

Claim 5: The driver circuit of claim 3, further comprising:

a signal line coupled to said output; and

a receiver coupled to said signal line;

wherein said capacitor of the first non-persistent charge boost circuit has a value that is at least twice the sum of i) the capacitance of the signal line, and ii) the gate capacitance of the receiver.

Claim 6 (canceled)

Claim 7: The driver circuit of claim 1, wherein the first switching circuit comprises a field effect transistor, the source and drain of which are coupled in said first current path, and the gate of which receives said input signal.

Claim 8: The driver circuit of claim 1, further comprising:

a signal line coupled to said output;

a receiver coupled to said signal line; and

a voltage clamp, coupled to said signal line in proximity to said receiver, to prevent a voltage at said receiver from reaching said first voltage.

Claim 9: The driver circuit of claim 1, further comprising:

a second current path coupled to a second voltage;

a second switching circuit, under control of said input signal, to couple and uncouple said second current path to said output;

a second current clamp, coupled in the second current path, to prevent a voltage at said output from reaching said second voltage; and

a second non-persistent charge boost circuit, coupled to the second switching circuit, to increase a rate at which said output switches toward said second voltage when said second current path is coupled to said output.

Claim 10: The driver circuit of claim 9, further comprising a second delay circuit, coupled to the output of the driver circuit, wherein:

the second non-persistent charge boost circuit comprises a second field effect transistor that is coupled in the second current path via its source and drain terminals; and

the gate of the second field effect transistor is coupled to an output of the second delay circuit.

Claim 11: The driver circuit of claim 9, wherein:

the second non-persistent charge boost circuit comprises a second field effect transistor that is coupled in the second current path via its source and drain terminals; and

the gate of the second field effect transistor is coupled to the output of the delay circuit.

Claim 12: The driver circuit of claim 9, further comprising:

a signal line coupled to said output;

a receiver coupled to said signal line; and

first and second voltage clamps, coupled to said signal line in proximity to said receiver, to prevent a voltage at said receiver from reaching either of said first or second voltages.

Claim 13: The driver circuit of claim 1, wherein the first current clamp is coupled to the first non-persistent charge boost circuit to arm the first non-persistent charge boost circuit when the first current path is not coupled to said output.

Claim 14: A driver circuit, comprising:

a first current path coupled to a first voltage;

first switching means to couple and uncouple the first current path to an output of the driver circuit;

first current clamping means, coupled in the first current path, to prevent a voltage at the output of the driver circuit from reaching said first voltage;

delay means, coupled to the output of the driver circuit; and

first non-persistent charge boost means, to increase a rate at which the output of the driver circuit switches toward the first voltage when the first current path is coupled to the output of the driver circuit, wherein the charge boost means comprises a field effect transistor that is i) coupled in parallel with the first current clamping means via its source and drain terminals, and ii) has its gate coupled to an output of the delay means.

Claim 15 (canceled)

Claim 16: The driver circuit of claim 14, further comprising:

a second current path coupled to a second voltage;

second switching means to alternately couple and uncouple said second current path to said output;

second current clamping means, coupled in the second current path, to prevent a voltage at said output from reaching said second voltage; and

second non-persistent charge boost means, coupled to the second switching means, to increase a rate at which said output switches toward said second voltage when said second current path is coupled to said output.

Claim 17: A method, comprising:

under control of an input signal, driving a signal line toward a first voltage by coupling a first current path to the signal line;

while the first current path is coupled to the signal line,

i) clamping current flow through the signal line, by means of a series-connected resistor in the first current path, to prevent the voltage on the signal line from reaching the first voltage; and

ii) providing a non-persistent charge boost to the signal line, by means of a field effect transistor that is i) coupled in parallel with said resistor via its source and drain terminals, and ii) has a gate that is driven by a delayed version of the voltage on the signal line, to increase a rate at which a voltage on the signal line switches toward said first voltage.

Claim 18: The method of claim 17, further comprising clamping voltages at a receiving end of the signal line to a range of voltages that is smaller than a range of voltages allowed at a driven end of the signal line.

Claim 19: The method of claim 17, further comprising:

under control of said input signal, driving said signal line toward a second voltage by uncoupling the first current path from the signal line and coupling a second current path to the signal line;

while the second current path is coupled to the signal line,

i) providing a non-persistent charge boost to the signal line, to increase a rate at which the voltage on the signal line switches toward said second voltage; and

ii) clamping current flow through the signal line to prevent a voltage on said signal line from reaching said second voltage.

Claim 20: The method of claim 19, further comprising clamping voltages at a receiving end of the signal line to a range of voltages that is smaller than a range of voltages allowed at a driven end of the signal line.

Claim 21: The method of claim 17, wherein, when the first current path is uncoupled from the signal line, the method used to clamp current provides a means to arm the charge boost.

Claim 22 (canceled)

Claim 23: The method of claim 22, wherein said non-persistent charge boost is further provided by a capacitor, coupled in parallel with said resistor.

Claim 24 (canceled)

Evidence Appendix

None.

Related Proceedings Appendix

None.